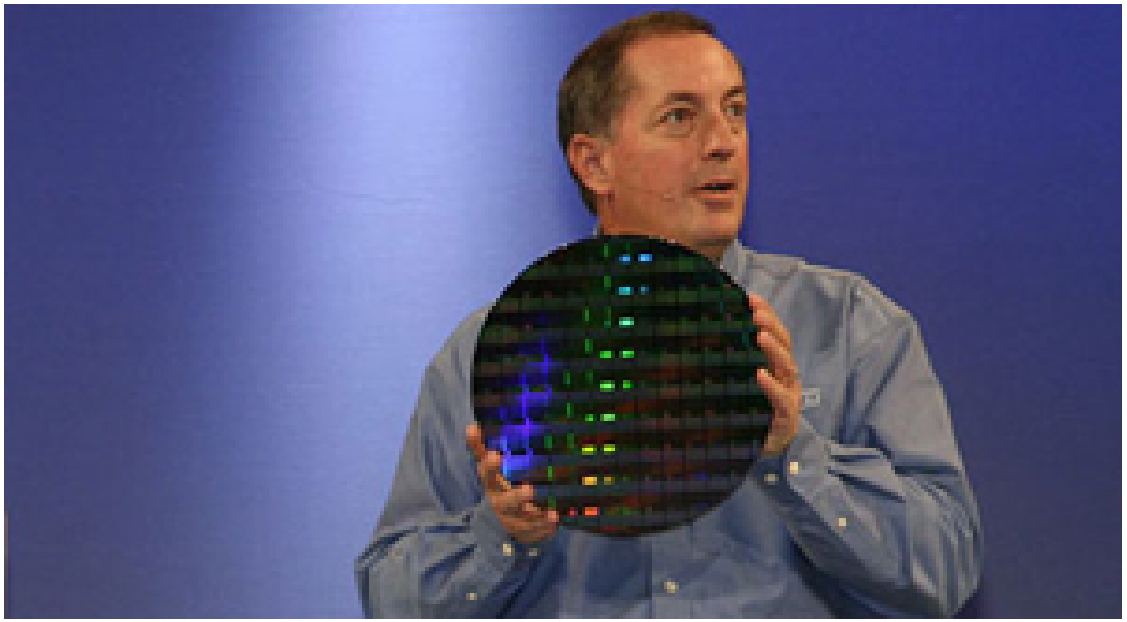
Intro to Chemical Vapor Deposition (CVD) in Semiconductor Fabrication



Paul Otellini, Intel CEO and President (ca. 2012) is holding a 300 mm-diameter wafer of single-crystal Si that has been patterned with hundreds of identical integrated circuits. CVD is one process used in the production of the circuits.

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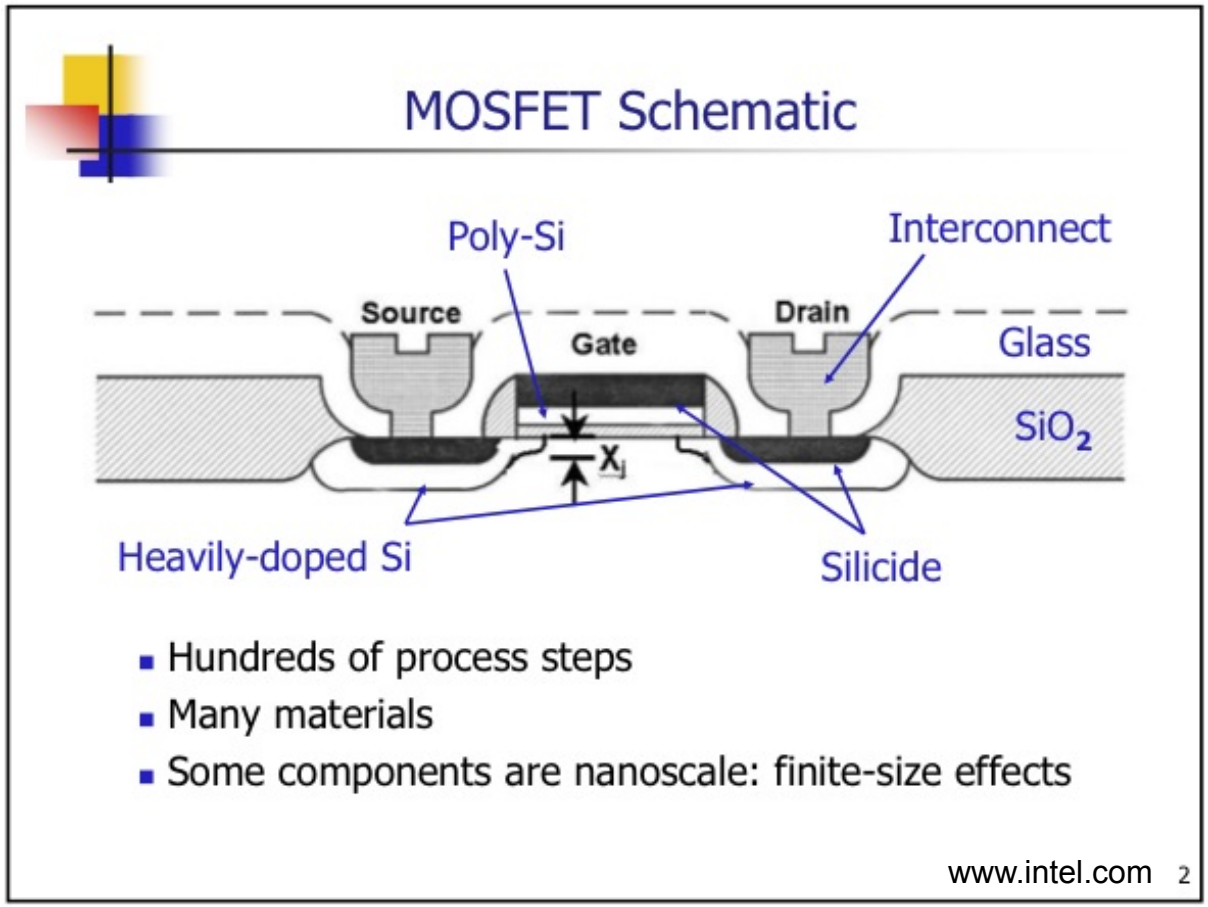
Questions? Contact Richard K. Herz, herz@ucsd.edu

Thin layers are patterned



This is an enlarged cross section of a transistor circuit as a thin pattern of materials on the surface of a wafer. The horizontal dimension is on the order of 100's of nm. To the bottom is the bulk of the Si wafer. Layers such as SiO_2 and polycrystalline Si are grown on the wafer and then patterned by photolithography. See Intel's From Sand to Silicon, The Making of a Chip <http://newsroom.intel.com/docs/DOC-2476>. Paper, colored ink and printing are to magazines as are Si wafers, elements such as B and P, and photolithography are to integrated circuits.

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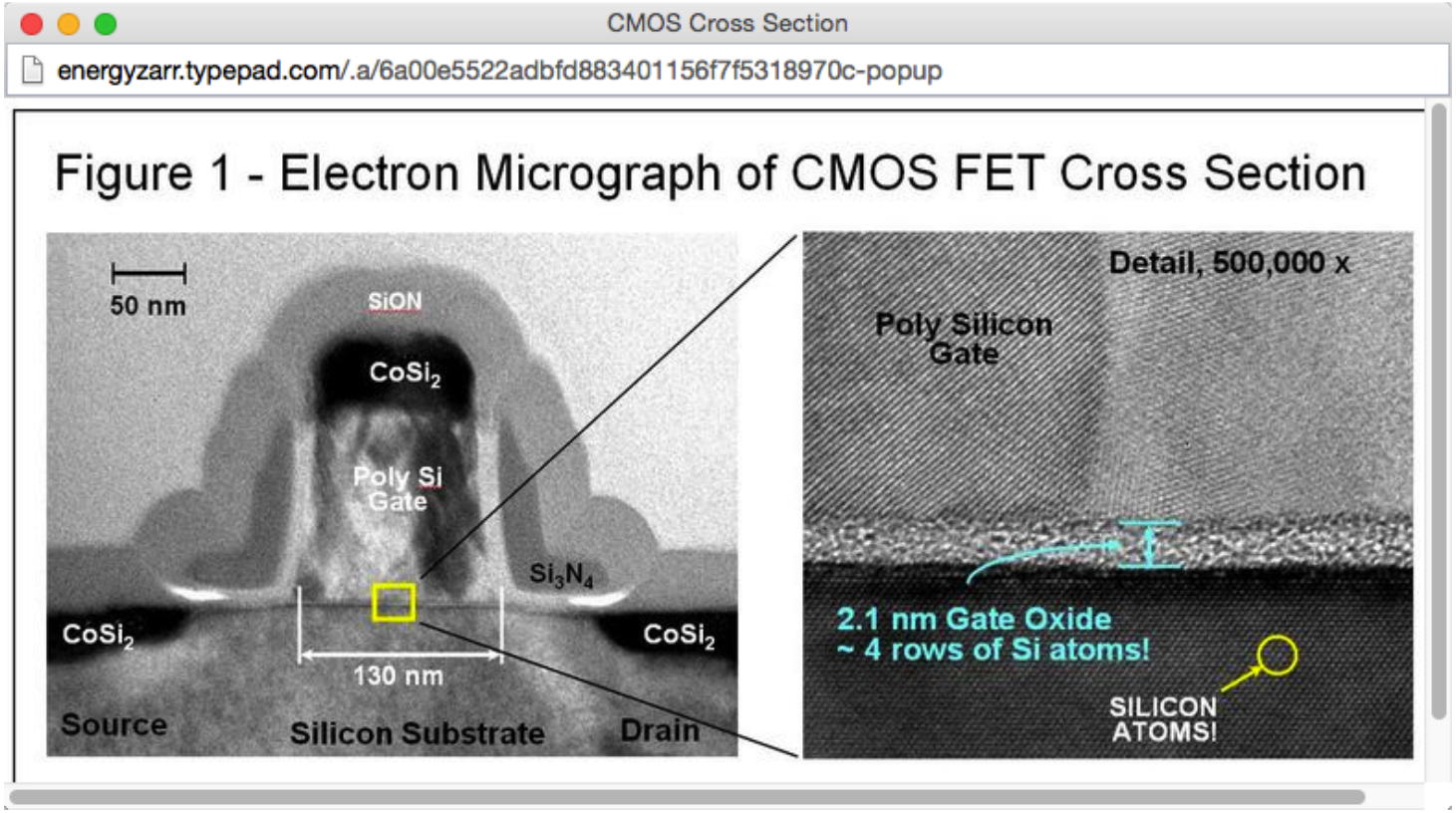

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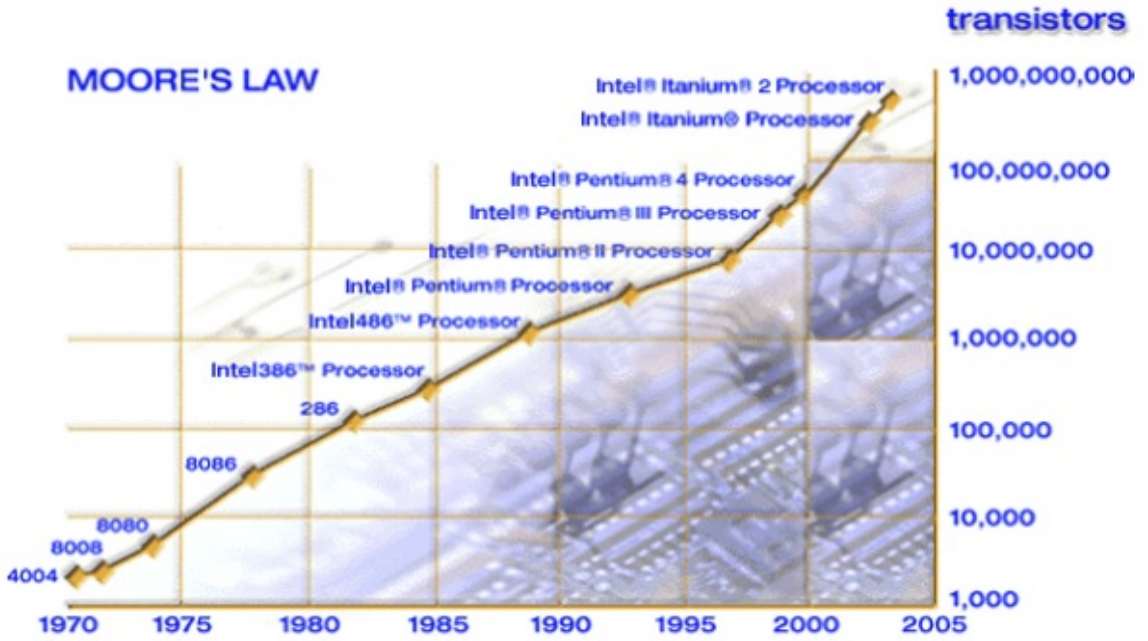
Transistor Scaling



Symbiosis with software industry:

Better hardware

Frillier software

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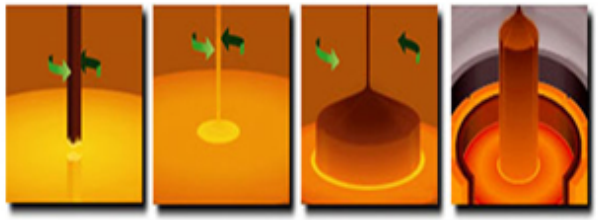
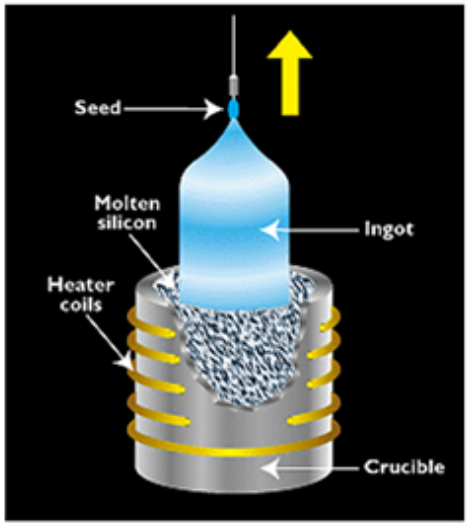
As the technology improves, the dimensions of circuit elements keep getting smaller so they can pack more transistors per unit area over the wafer surface. "Frillier" software, haha! They must be referring to Microsoft Office's "ribbon."

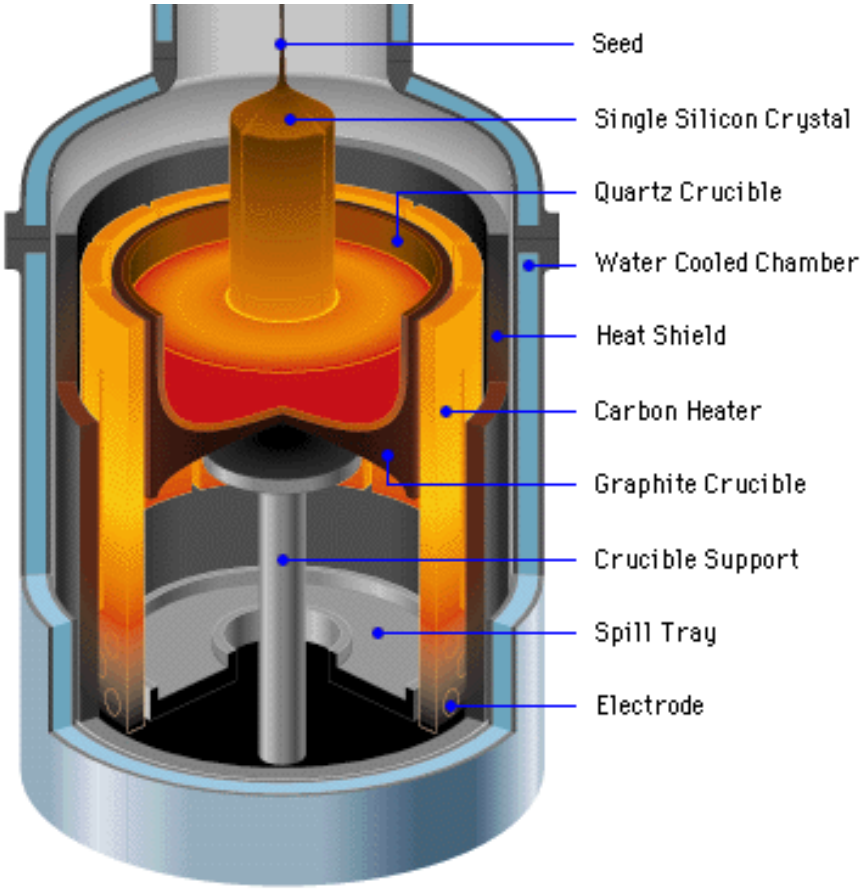
Wafers are cut from single crystals





Si orginates by reducing "sand" (SiO_2) by reaction with carbon. This makes relatively impure metallurgical grade Si. This is further purified by reacting the Si and C impurities with HCl, separating the resulting chloride gas products by distillation, and then decomposing them back to Si solid. This is then melted and a large cylindrical single crystal is pulled slowly from the melt in the Czochralski method.

Czochralski furnace



people.seas.harvard.edu/~jones/es154

Hanging by a thread!

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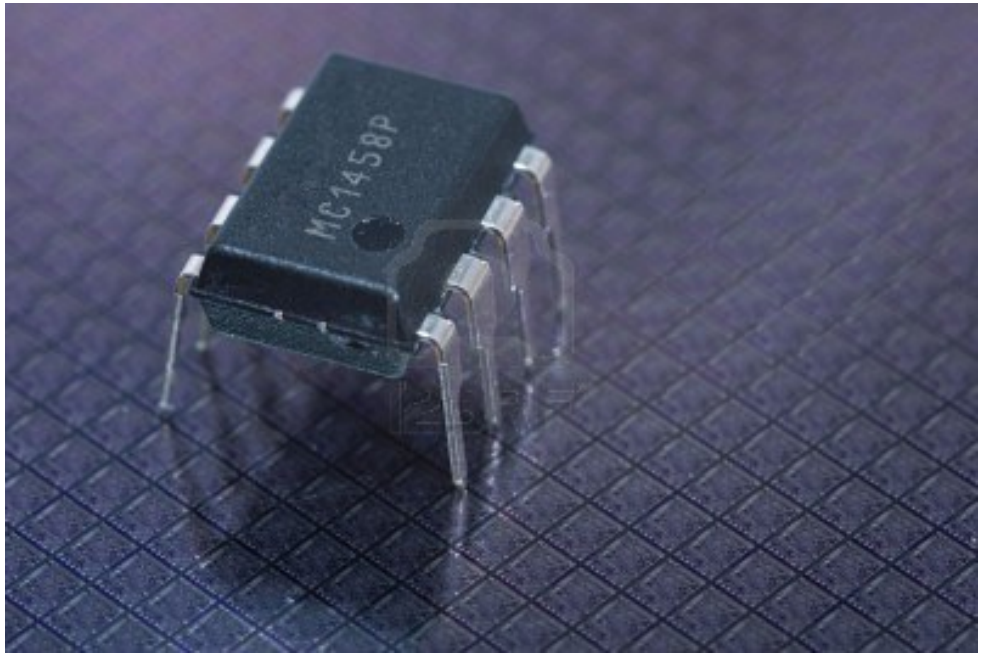
Fig. 7 Person with lint-free garments in a vertical laminar-flow clean room for integrated-circuit fabrication with 300-mm (12-in.) wafer. (Personnel do not handle wafers in this manner. This was done just for the photograph.) (*Intel Corp.*)

The large cylindrical single crystals of Si are cut into thin wafers with a wire saw and then polished.

Chips cut & packaged



This shows a wafer surface with many identical electronic circuits that have been patterned over its surface. The finished wafer is cut into individual elements, then each circuit element is packaged into a chip that can be plugged into a circuit board.

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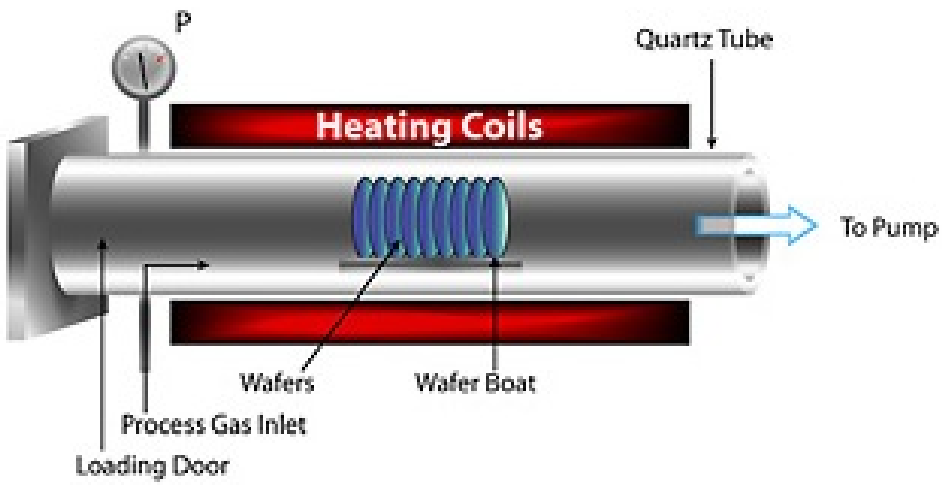
A variety of CVD processes are used

LPCVD (Low Pressure)

This technique permits either horizontal or vertical loading of the wafers into the furnace and accommodates large numbers of wafers for processing. It gives good conformal-step coverage with excellent purity and uniformity (typically better than APCVD and PECVD). There is less dependence of the resulting layer on gas flow. However, the process requires higher temperatures and the deposition rate is low. Pressures required can be from 0.1 to 2 torr.

LPCVD System



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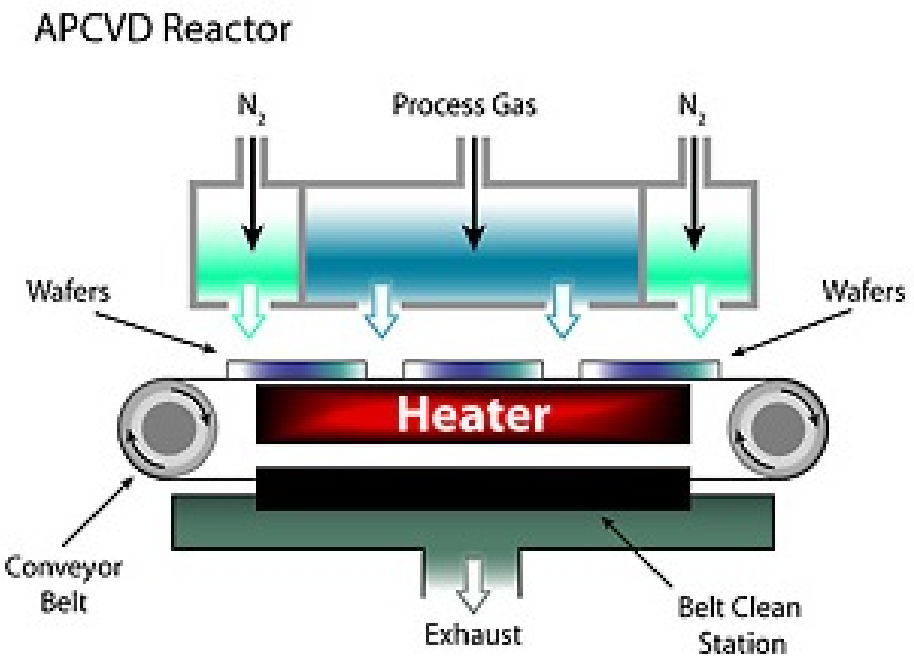
LPCVD furnace & wafers

Low pressure CVD is used to grow the first layer of SiO_2 over the Si wafer surface. The flat cut on the wafer edge indicates the crystalline orientation of the wafer. Wafers are loaded into quartz holders ("boats") and then inserted into a quartz reactor tube in a furnace. The goal is to grow the layer to a uniform thickness across the diameter of each wafer and from wafer to wafer from the reactor inlet to its outlet. To a first approximation, the math is similar to that for reaction over porous catalyst pellets in a packed-bed reactor. Can you see why?

A variety of CVD processes are used

APCVD (Atmospheric Pressure)

This is a relatively simple system that can operate with wafers on a horizontal conveyor belt. Deposition rate is fast and at low temperatures. The use of this method with ozone and TEOS is common in the industry, especially for shallow trench and pre-metal deposition layers.



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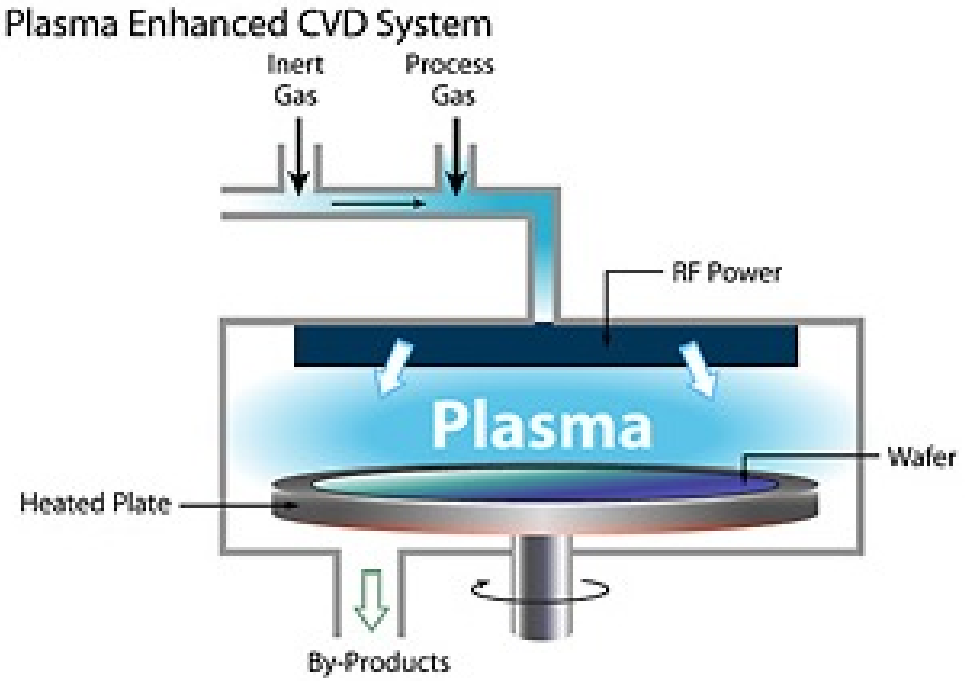
A variety of CVD processes are used

PECVD (Plasma Enhanced)

In this process, radio frequency (RF) is used to induce plasma in the deposition gas. This results in a higher deposition rate at relatively low temperatures. Step coverage is good.



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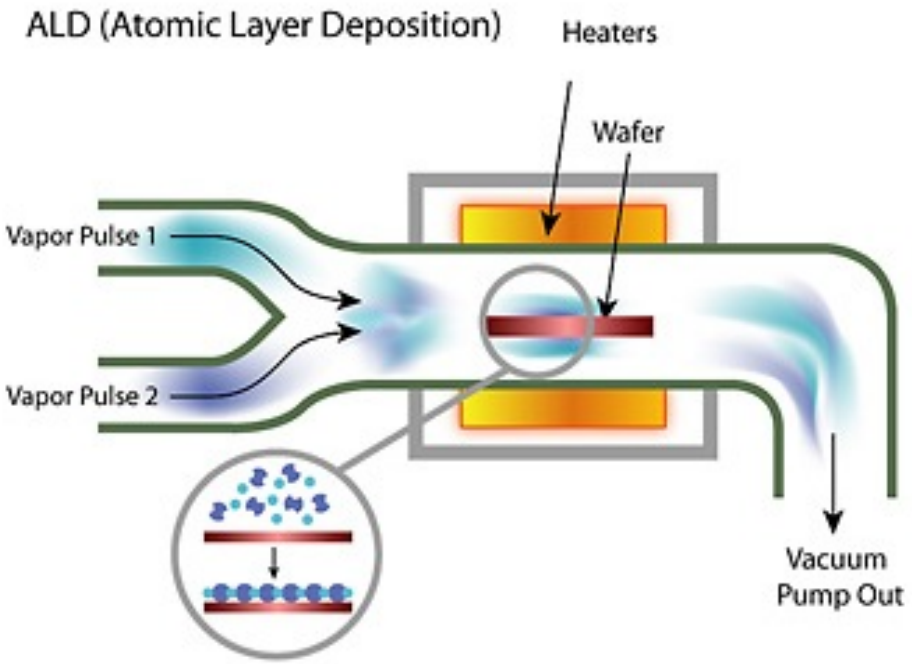
A variety of CVD processes are used

ALD (Atomic Layer Deposition)

Relatively new as a commercially available technique, ALD utilizes sequential precursor gas pulses to deposit a film one layer at a time. The first precursor gas is introduced into the process chamber and produces a monolayer of gas on the substrate. A second precursor gas is then introduced into the chamber and reacts with the monolayer produced from the first gas. Since each pair of gas pulses (which is one cycle) produces exactly one monolayer of the desired film, the thickness of the final film is precisely controlled by the number of deposition cycles.



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